Analog Integrated Circuit Design Automation

AIDA assists expert analog IC designers by automating the most time-consuming and repetitive tasks from the typical analog IC design flow.

- **AIDA-C** automates circuit sizing with high accuracy and within a reduced time frame.
- **AIDA-L** generates the complete layout for sized circuits, from device placement to detailed routing.

RECENT AWARDS

- **SMACD 2015**
  1st Ranked on “Design Automation Competition”
- **IEEE ISCAS 2014**
  Best Paper Award Runner-Up

RELATED PUBLICATIONS

- DATE 2016, DATE 2015, DATE 2014, IEEE ISCAS 2015, IEEE ISCAS 2014, IEEE TCAD, Integration, the VLSI Journal, ESWA Journal

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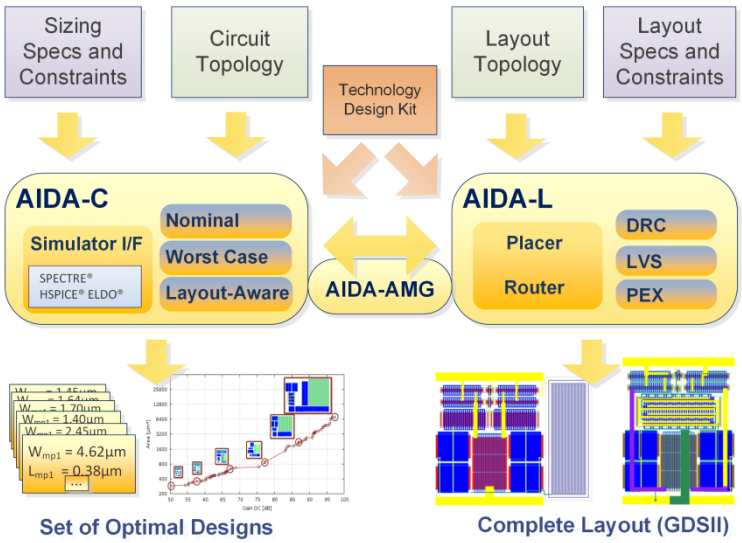
AIDAsoft

Analog IC Design Automation

The Analog IC Design Automation (AIDA) framework implements an analog IC design flow from circuit-level specification to a physical layout description focusing on design optimizing and porting using highly efficient searching methods combined with accurate circuit-level simulation, layout design rules and parasitic extraction engines.



Analog and Mixed-Signal (AMS) systems are found in a wide range of applications, such as, communications, medical or multimedia applications. These extremely competitive markets force the analog designer to face the complex design challenges within strict and demanding time frames.

Today’s analog design is supported by circuit simulators, layout editing environments and verification tools, however the design cycle for AMS ICs is still long and error-prone.

AIDA’s framework targets the analog IC design automation while keeping the common design flow by involving the designer’s knowledge and focusing on efficiently automating repetitive design tasks. Thus, facilitating design reuse and fast response to specification changes of analog cells like VCO, LNA, voltage mixer, differential amplifiers, band gap voltage references, integrators, comparators, etc..

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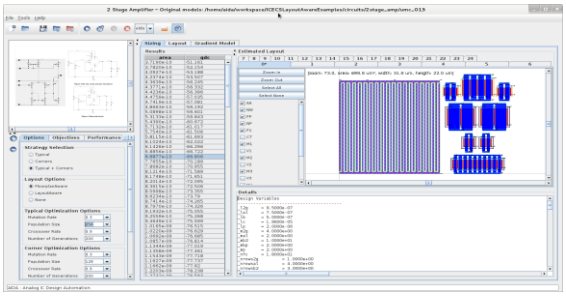
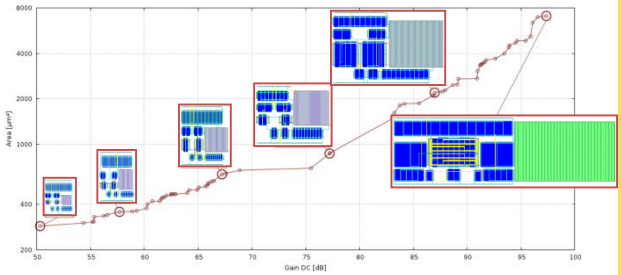
AIDA framework is composed by two main modules: **AIDA-C** and **AIDA-L**. AIDA also includes an intuitive GUI allowing the designer to manage and interact with the design automation process.



AIDA's Graphical User Interface navigating on the sizing solution set and showing the corresponding floorplan.

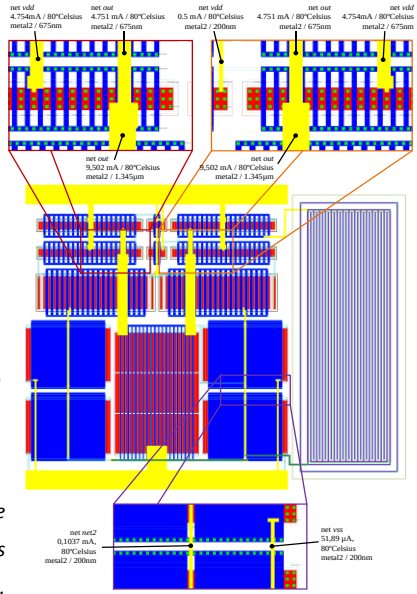
AIDA-C is the circuit-level synthesizer supported by state-of-the-art multi-objective optimization kernels, where the robustness of the solutions is attained by considering user-defined worst case corners, that account for process variations and(or) PVT corners. The circuit's performance is measured using **Spectre®**, **Eldo®** or **HSPICE®** electrical circuit simulators.



Pareto optimal solution set for Area vs. DC Gain optimization with superimposed circuit layouts.

AIDA-L generates the complete layout of the sized circuit by placing and, routing the devices, while fulfilling the technology design rules by using built-in DRC and LVS procedures. The router takes into account the circuit's currents to mitigate electromigration and IR-drop effects, and a fast but accurate PEX procedure provides parasitic estimates to be used in **AIDA-C** layout-aware optimization.

The framework's technology independent module generator, **AIDA-AMG**, is capable of creating several, simple and complex, device layout styles, allowing **AIDA-C** floorplan-aware sizing approach to explore a much wider space of solutions leading to higher quality layouts.



Complete layout detailing the connections where EM effects caused wires width to increase.

AIDA Features

- Fully automatic design or semi-automatic allowing designer intervention.
- Supported System: Linux Fedora 16, Linux RedHatEnterprise 5.8
- Uses standard electrical circuit simulators as evaluation engines.
- Handles multiple circuit test-benches simultaneously.
- Provides a Pareto optimal front of circuit sizing solutions showing the trade-offs among the design objectives.
- Semi-automatic template generation from netlist.
- Template-based floorplanner with symmetry and automatic proximity constraints.
- Electromigration and IR-drop aware symmetric routing.
- Fast PEX enables layout-aware circuit-level multi-objective multi-constraint optimization.
- Includes a technology independent analog module generator to enrich floorplan solutions.

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